TITLE OF THE INVENTION

ADD/DROP CROSS CONNECTION APPARATUS FOR SYNCHRONOUS DIGITAL HIERARCHY

CLAIM OF PRIORITY

[0001] This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C §119 from an application entitled *Add/Drop Cross Connection Apparatus For Synchronous Digital Hierarchy* earlier filed in the Korean Industrial Property Office on 10 January 2000, and there duly assigned Serial No. 2000-897 by that Office.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a synchronous digital hierarchy system (SDH System), and more particularly to an add/drop cross connection apparatus for an SDH system.

Description of the Related Art

[0003] Cross-connects are electronic multiport switches for digital traffic and are known in the United States as digital cross-connect switches (DCSs) and as DXCs elsewhere. They are classified

as DCS p/q or DXC p/q, where p is the hierarchical order of a port bit rate and q is the hierarchical order of the traffic component that is switched within that port bit rate.

[0004] DXC/DCS can occur in two main types. Higher order cross-connects, generally used to route bulk traffic in blocks of nominally 155 MBPS for network provisioning or restoration, and are designated as DXC 4/4. Lower order cross-connects (DXC 4/1, or 1/1) are used for time switching leased lines, consolidation, and service restoration.

[0005] In an add/drop cross connection apparatus of an exemplary SDH system, the data supplied from a west or east aggregate unit is divided into lower and the higher order path data. The lower order path data (or lower order virtual container (VC)) may be TU11 (Tributary Unit 11) or TU12 data processed by a TU pointer while the higher order path data (or higher order virtual container) may be AU3 (Administrative Unit 3) or AU4 data and has an AU pointer.

[0006] The lower order path data supplied from the west or east aggregate unit is matched to the system clock through a multiplex section adaptation circuit and supplied to a higher order path overhead monitor circuit. The higher order path overhead monitor circuits respectively monitors the higher order path overheads of the data respectively supplied from the multiplex section adaptation circuits, which are then delivered to the higher order path connection circuit. The higher order path connection circuit performs the cross connection to the lower order path data by space switching and supplying the lower order path data to the lower order path data processor, which performs the cross connection to the data, aligns the data, and detects and monitors various path overheads. The data processed by the lower order path data processor is delivered to a lower order tributary device.

[0007] Meanwhile, the higher order path data supplied from the west or east aggregate unit and

supplied to the higher order path overhead monitor circuit is matched to the system clock through the multiplex section adaptation circuit. The higher order path overhead monitor circuit respectively monitors the higher order path overheads of the data respectively supplied from the multiplex section adaptation circuits and delivers the higher order path data to the higher order path connection circuit. The higher order path connection circuit performs the cross connection to the higher order path data by space switching and supplies the higher order path data to a higher order tributary device, which may be a known device such as DS3 (Digital Signal Level 3 of 44.736 MBPS), OC-1 (Optical Carrier supporting a Synchronous Transport Signal, Level 1 of 51.840 MBPS), STM-1 (Synchronous Transport Module, Level 1 of 155.520 MBPS) or STM-4 (Synchronous Transport Module, Level 4 of 622.080 MBPS) equipment. The SDH system is based upon the fundamental STM-1 rate, which is three times the fundamental SONET (Synchronous Optical NETwork) rate. The typical transmission media is defined to be an optical fiber, but the Broadband ISDN specification does define a User-Network Interface (UNI) STM-1 operating over coaxial cables.

[0008] In addition, the lower order path data supplied from the lower order tributary device is subjected through the lower order path data processor to the cross connection by time switching and delivered to the higher order path connection circuit. The higher order path connection circuit subjects the input data to cross connection by space switching and then supplies the data via a higher order unequipped generator to the west or east aggregate units. Meanwhile, the higher order path data supplied from the higher order tributary device is subjected through the higher order path connection circuit to cross connection by space switching and delivered through the higher order unequipped generator to the west or east aggregate units.

[0009] Hence, such add/drop cross connection apparatus is so complicated as to have one connecting path connecting it to the lower order tributary device and to separately have a second connecting path connecting it to the higher order tributary device.

[0010] Incorporated by reference herein are: U.S. Patent No. 6,094,440 to Toshiki Sugawara et al. entitled *Multiplex Type Transmitting Apparatus*; U.S. Patent No. 5,914,952 to Doo Seop Eom et al. entitled *Tributary Unit Signal Cross-Connection Apparatus*; U.S. Patent No. 5,799,001 to Dong Choon Lee et al. entitled *Composite Network Protective/Recovering Device For Synchronous Digital Hierarchy DXC*; U.S. Patent No. 5,777,998 to Giovanni Traverso et al. entitled *Method And Circuit Arrangement For The Realization Of The Higher Path Adaptation/Mapping Function In Synchronous Digital Hierarchy/Optical Network Equipment*; U.S. Patent No. 5,574,717 to Masahito Tomizawa et al. entitled *Line Terminating Equipment In SDH Networks, Using Forward Error Correcting Codes*; and U.S. Patent No. 5,555,248 to Eiji Sugawara entitled *Tandem Connection Maintenance System*.

SUMMARY OF THE INVENTION

[0011] It is an object of the present invention to provide an add/drop cross connection apparatus of an SDH system that is simplified by combining the path connecting the lower order tributary device and the path connecting the higher order tributary device.

[0012] According to an aspect of the present invention, an add/drop cross connection apparatus of an SDH system, comprises an aggregate unit matching device for providing matching with the aggregate units, a higher order path connection circuit for subjecting received higher order path data

to cross connection by space switching, a lower order path connection circuit for subjecting received lower order path data to cross connection by space switching, and a selector for selectively delivering the data supplied from the aggregate units, higher order tributary device, and lower order tributary device, wherein the selector delivers the data to the higher order path connection circuit or lower order path connection circuit according to whether the data is the higher or lower order path data.

[0013] The present invention will now be described more specifically with reference to the drawings attached only by way of example.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

[0014] A more complete appreciation of the present invention, and many of the attendant advantages thereof, will become readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

[0015] Fig. 1 is a block diagram for illustrating the structure of a complicated add/drop cross connection apparatus of an SDH system; and

[0016] Figs. 2 to 6 are block diagrams for illustrating the add/drop cross connection apparatus of an SDH system according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0017] Throughout descriptions in connection with the drawings, same reference numerals are

used to represent same functional parts for convenience s sake. In addition, there are omitted detailed descriptions of the conventional parts not required to comprehend the technical concept of the present invention.

[0018] Referring to Fig. 1 for illustrating the structure of the add/drop cross connection apparatus of an SDH system, the data supplied from the west or east aggregate unit is divided into the lower and the higher order path data. The lower order path data is TU11 (Tributary Unit 11) or TU12 data processed by a TU pointer while the higher order path data is AU3 (Administration Unit 3) or AU4 data.

[0019] The lower order path data supplied from the west or east aggregate unit is matched to the system clock through the multiplex section adaptation (MSA) circuits 100 or 102, and supplied to the higher order path overhead monitor (HPOM) circuits 104 or 106. The HPOM circuits 104 and 106 respectively monitor the higher order path overheads of the data respectively supplied from the MSA circuits 100 and 102, which are delivered to the higher order path connection (HPC) circuit 108. The HPC circuit 108 performs the cross connection to the data by space switching, and supplies the data to the lower order path data processor 110, which performs the cross connection to the data, aligns the data, and detects and monitors various path overheads. The data processed by the lower order path data processor 110 is delivered to the lower order tributary device.

[0020] Meanwhile, the higher order path data supplied from the west or east aggregate unit is matched to the system clock through MSA circuits 100 or 102, and supplied to the HPOM circuits 104 or 106. The HPOM circuits 104 and 106 respectively monitor the higher order path overheads of the data respectively supplied from the MSA circuits 100 and 102, and delivers the data to HPC

circuit 108. The HPC circuit 108 performs the cross connection to the data by space switching, and supplies the data to the higher order tributary device, which may be DS3, OC-1, STM-1 or STM-4 equipment.

[0021] In addition, the lower order path data supplied from the lower order tributary device is subjected through the lower order path data processor 110 to the cross connection by time switching, and delivered to the HPC circuit 108. The HPC circuit 108 subjects the input data to cross connection by space switching, and delivers the data through the higher order unequipped generators (HUG) 112 or 114 to the west or east aggregate units. Meanwhile, the higher order path data supplied from the higher order tributary device is subjected through the HPC circuit 108 to cross connection by space switching, and delivered through HUGs 112 or 114 to the west or east aggregate units.

[0022] Hence, such add/drop cross connection apparatus is so complicated as to have one connecting path connecting it to the lower order tributary device and to separately have a second connecting path connecting it to the higher order tributary device.

[0023] Referring to Fig. 2, MSA circuits 200 and 202 respectively match the data received from the west and east aggregate units to the system clock through pointer processing. The data is then delivered to the respective HPOM circuits 204 and 206, which detect and monitor the higher order overheads to be delivered to the HPC circuit 208. The HUG circuits 226 and 228 generate unequipped signals to transfer the data from the HPC circuit 208 to the west or east aggregate unit. The MSA circuits 200 and 202, HPOM circuits 204 and 206, and HUGs 226 and 228 constitute the aggregate unit matching device to provide matching with the aggregate units.

[0024] The HPC circuit 208 comprises an HPC device 210 and a selector 212. The HPC device

210 performs cross connection by space switching to the data supplied from the HPOM circuits 204 and 206, lower order path data processor 214, or higher order tributary device. The selector 212 selectively delivers the input data to the lower order path data processor 214, lower order tributary device, high order tributary device, or HPC device 210, which is initially determined by the operator.

[0025] The lower order path data processor 214 comprises a higher order path termination (HPT) circuit 216 for processing POH of VC3/VC4, higher order path adaptation (HPA) circuit 218 for aligning data by unit of TU11 or TU12, lower order path overhead monitor (LPOM) circuit 220 for detecting known path overhead bytes (J2 (path trace signal), V5 (BIP-2: a bit interleaved parity operation), etc.), lower order unequipped generator (LUG) 224 for generating unequipped signals by unit of VC11 or VC12, and lower order path connection (LPC) circuit 222 for performing cross connection by time switching to TU11 or TU12 signals.

[0026] Describing transference of data in the add/drop cross connection apparatus, the tributary device of DS1 (1.544 MBPS) or DS1E (3.152 MBPS) equipment inputs the lower order path data TU11 or TU12 subjected to TU pointer processing to the selector 212 in order to deliver it to the west aggregate unit. Then, the selector 212, as shown by the dash-dot-dash line in Fig. 2, delivers the input data through LPOM circuit 220 to LPC circuit 222 to LUG 224 to HPT circuit 216 to HPC device 210 to HUG circuit 226 to the west aggregate device.

[0027] In addition, the tributary device of DS3, OC-1, STM-1 or STM-4 equipment inputs the higher order path data AU3 or AU4 to the selector 212 to deliver it to the west aggregate unit. Then, the selector 212, as shown by the dash-dash-dash line in Fig. 2, delivers the input data through HPC device 210 to HUG circuit 226 to the west aggregate. Accordingly, selector 212 routes the data

based on whether the data is received from a high order tributary device or a low order tributary device. That is, selector 212 is a kind of space switching apparatus for selecting a path of TU11 / TU11 (DS1/DS1E Interface Equipment) and VC3 / VC4 (DS3 / STM-1 / STM-4 Interface Equipment). The selector does not discriminates the input date by using an any other specific method but select whether or not the input data is transmitted by way of HPT, HPA in response to a determination of whether the input data is input through the low speed interface apparatus (DS1 / DS1E) or the high speed interface apparatus (DS3/ STM-1 / STM-4).

[0028] In addition, the tributary device of DS3, OC-1, STM-1 or STM-4 equipment inputs the higher order path data AU3 or AU4 subjected to lower order path cross connection to the selector 212 to deliver it to the west aggregate unit. Then, the selector 212, as shown by the dash-dot-dash line in Fig. 3, delivers the input data through HPC device 210 to HPT 216 to HPA circuit 218 to LPOM circuit 220 to LPC circuit 222 to LUG circuit 224 to HPT circuit 216 for lower order path crossing, finally through HPC device 210 to HUG circuit 226 and then to the west aggregate unit. The HPC device routes the data according to the known ITU Standard G.783.

[0029] When the west aggregate unit delivers the lower order path data to the tributary device of DS1 or DS1E equipment, the data input through MSA circuit 200 to HPOM circuit 204 is delivered through HPC device 210 to selector 212, which, as shown by the dash-dash-dash line in Fig. 4, delivers the data through HPT circuit 216 to HPA circuit 218 to LOPM circuit 220 to LPC circuit 222. Finally, the selector 212 delivers the data received from the LPC circuit 222 to the lower order tributary device.

[0030] In addition, the west aggregate unit delivers the higher order path data through MSA circuit

200 to HPOM circuit 204 to HPC device 210 to selector 212 to the higher order tributary device of DS3, OC-1, STM-1 or STM-4 equipment, as shown by te dash-dot-dash line in Fig. 4.

[0031] When the west aggregate unit sends the higher order path data to the east aggregate unit, the input data, as shown by the dash-dot-dash line in Fig. 5, is delivered through MSA circuit 200 to HPOM circuit 204 to HPC device 210 to HUG circuit 228 to the east aggregate unit.

[0032] In addition, when the west aggregate unit sends the lower order path data to the east aggregate unit, the input data, as shown by the dash-dash-dash line in Fig. 5, is delivered through MSA circuit 200 to HPOM circuit 204 to HPC device 210 to HPT circuit 216 to HPA circuit 218 to LOPM circuit 220 to LPC circuit 222 to LUG circuit 224 to HPT circuit 216 to HPC device 208 and, finally, through HUG circuit 206 to the east aggregate unit.

[0033] In addition, the lower order path data input from the lower order tributary device to the selector 212, as shown by the dash-dash-dash line in Fig. 6, is delivered through LPOM circuit 220 to LPC circuit 222 to LUG circuit 224 to the selector 212, returning to the lower order tributary device.

[0034] In addition, the higher order path data input from the higher order tributary device to the selector 212, as shown by the dash-dot-dash line in Fig. 6, is delivered through HPC device 210 to the selector 212, returning to the higher order tributary device.

[0035] Thus, the invention provides the HPC circuit 208 with the selector 212 so that the lower order data passes the lower order data processor to the tributary devices or aggregate units along the path determined by the user. Hence, the path for the lower order tributary device and the path for the higher order tributary are converged to the path through the selector 212, simplifying the structure

of the add/drop cross connection apparatus.

[0036] While the present invention has been described in connection with specific embodiments accompanied by the attached drawings, it will be readily apparent to those skilled in the art that various changes and modifications may be made thereto without departing the gist of the present invention.